

## N and P Channel 40V MOSFET

### GENERAL DESCRIPTION

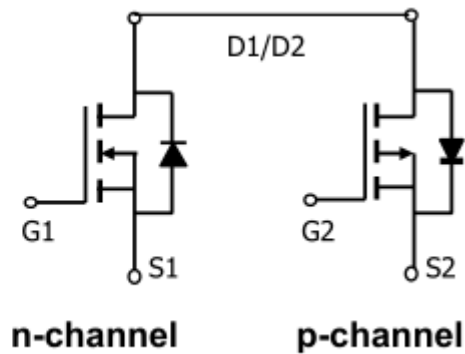
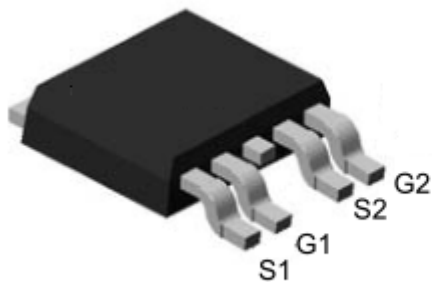
The JY13M is the N and P Channel logic enhancement mode power field transistors Which can provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

### FEATURES

Device	$V_{BR(DSS)}$	$R_{DS(ON) MAX} T_J=25^{\circ} C$	Package
N-Channel	40V	$<30m\Omega @ V_{GS}=10V, I_D=12A$	TO252-4L
		$<40m\Omega @ V_{GS}=4.5V, I_D=8A$	
P-Channel	-40V	$<45m\Omega @ V_{GS}=-10V, I_D=-12A$	
		$<66m\Omega @ V_{GS}=-4.5V, I_D=-8A$	

- Low Input Capacitance
- Fast Switching Speed

### PIN CONFIGURATION



# JY13M

## Absolute Maximum Ratings(Ta=25° C Unless Otherwise Noted)

Parameter		Symbol	N Channel	P Channel	Unit
Drain Source Voltage		$V_{DSS}$	40	-40	V
Gate Source Voltage		$V_{DSS}$	$\pm 20$	$\pm 20$	
Continuous Drain Current	Ta=25° C	$I_D$	12	-12	A
	Ta=100° C		12	-12	
Pulsed Drain Current		$I_{DM}$	30	-30	
Maximum Power Dissipation	Ta=25° C	$P_D$	2		W
	Ta=70° C		1.3		
Junction and Storage Temperature Range		$T_J$ $T_{STG}$	-55 to 150		° C
Thermal Resistance Junction to Ambient		$R_{\theta JA}$	10s	25	°C/W
			Steady	60	
Thermal Resistance Junction to Case		$R_{\theta JC}$	5.5	5	°C/W

## Electrical Characteristics(Ta=25° C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Static</b>							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	N-Ch	1.7	2.5	3.0	V
		$V_{DS}=V_{GS}, I_D=-250\mu A$	P-Ch	-1.7	-2	-3.0	
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	N-Ch			$\pm 100$	nA
			P-Ch			$\pm 100$	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$	N-Ch			1	uA
		$V_{DS}=-40V, V_{GS}=0V$	P-Ch			-1	
$I_{D(ON)}$	On-State Drain Current	$V_{DS}=5V, V_{GS}=10V$	N-Ch	30			A
		$V_{DS}=-5V, V_{GS}=-10V$	P-Ch	-30			
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=12A$	N-Ch		24	30	mΩ
		$V_{GS}=-10V, I_D=-12A$	P-Ch		36	45	
		$V_{GS}=4.5V, I_D=8A$	N-Ch		31	40	
		$V_{GS}=-4.5V, I_D=-8A$	P-Ch		51	66	
$V_{SD}$	Diode Forward Voltage	$I_S=1.0A, V_{GS}=0V$	N-Ch		0.76	1.0	V
		$I_S=-1.0A, V_{GS}=0V$	P-Ch		-0.76	-1.0	

## Electrical Characteristics(Ta=25°C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Dynamic</b>							
Qg	Total Gate Charge	N-Channel V <sub>DS</sub> =20V,V <sub>GS</sub> =10V, I <sub>D</sub> =12A P-Channel V <sub>DS</sub> =-20V,V <sub>GS</sub> = -10V,I <sub>D</sub> =-12A	N-Ch		8.3	10.8	nC
			P-Ch		16.2	21	
Qgs	Gate-Source Charge		N-Ch		2.3		
			P-Ch		3.8		
Qgd	Gate-Drain Charge		N-Ch		1.6		
			P-Ch		3.5		
Ciss	Input Capacitance	N-Channel V <sub>DS</sub> =20V,V <sub>GS</sub> =0V, f=1MHz P-Channel V <sub>DS</sub> =-20V,V <sub>GS</sub> =0V, f=1MHz	N-Ch		516	650	pF
			P-Ch		900	1125	
Coss	Output Capacitance		N-Ch		82		
			P-Ch		97		
Crss	Reverse Transfer Capacitance		N-Ch		43		
			P-Ch		68		
Rg	Gate Resistance	V <sub>DS</sub> =0V,V <sub>GS</sub> =0V, f=1MHz	N-Ch		4.6	Ω	
			P-Ch		14		
T <sub>d(on)</sub>	Turn-On Delay Time	N-Channel V <sub>DD</sub> =20V,V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω P-Channel V <sub>DD</sub> =-20V,V <sub>GS</sub> =-10 V, R <sub>G</sub> =3Ω	N-Ch		6.4	ns	
			P-Ch		6.2		
T <sub>r</sub>	Turn-On Rise Time		N-Ch		3.6		
			P-Ch		8.4		
T <sub>d(off)</sub>	Turn-Off Delay Time		N-Ch		16.2		
			P-Ch		44.8		
T <sub>f</sub>	Turn-Off Fall Time	N-Ch		6.6			
		P-Ch		41.2			
T <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =12A, di/dt=100A/us	N-Ch		18	ns	
			P-Ch		21		
Q <sub>rr</sub>	Reverse Recovery Charge		N-Ch		10	nC	
			P-Ch		14		

\*The device mounted on 1in2 FR4 board with 2oz copper.

\*Guaranteed by design. Not subject to product testing.

## Typical Characteristics ( $T_J=25^\circ\text{C}$ Noted)

## N-Channel

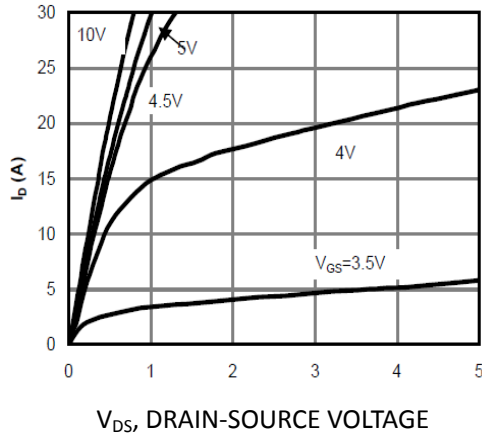


Figure 1. Typical Output Characteristic

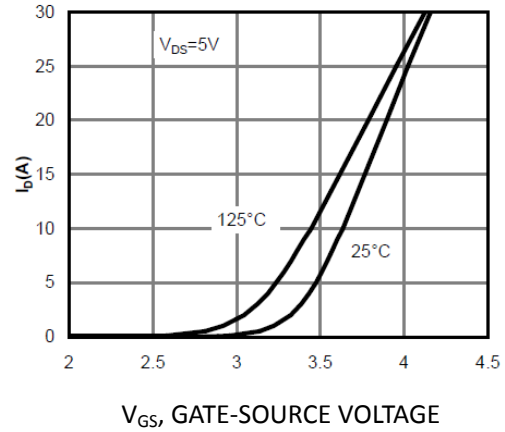


Figure 2. Typical Transfer Characteristics

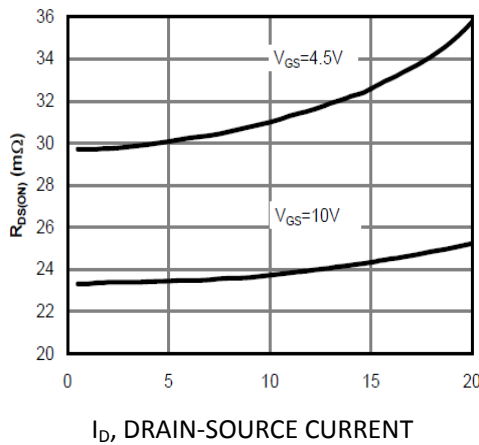


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

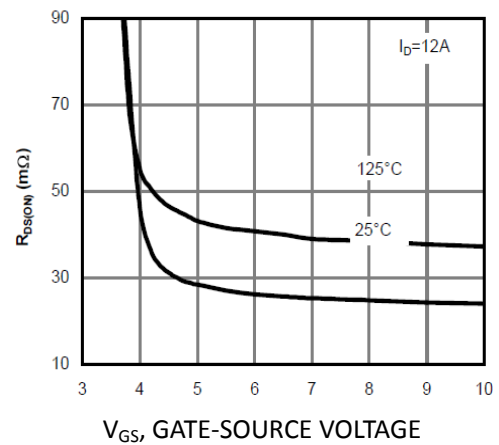


Figure 4. Typical On-Resistance vs. Drain Current and Gate Voltage

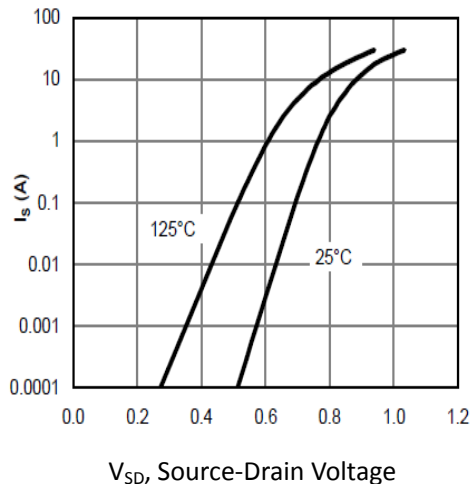


Figure 5. Body-Diode Characteristics

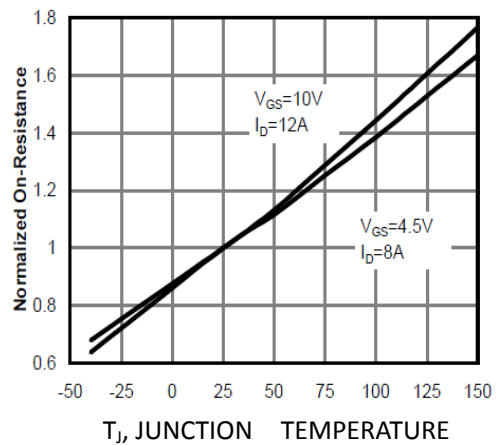


Figure 6. On-Resistance Variation with Temperature

## Typical Characteristics ( $T_J=25^\circ\text{C}$ Noted)

## N-Channel

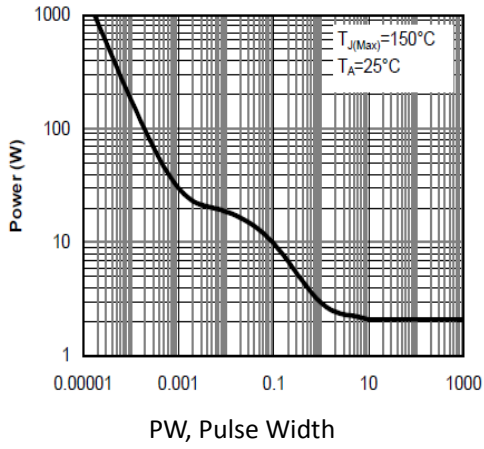


Figure 9. Single Pulse Power Rating  
Junction-to-Ambient

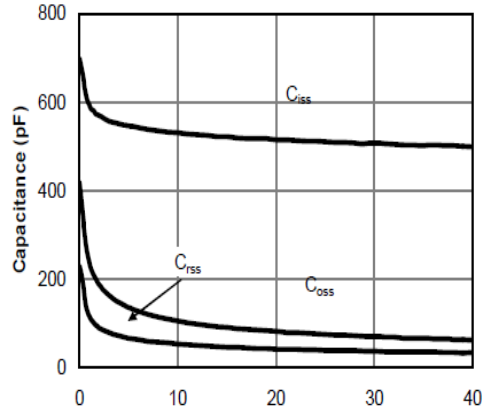


Figure 10. Typical Junction Capacitance

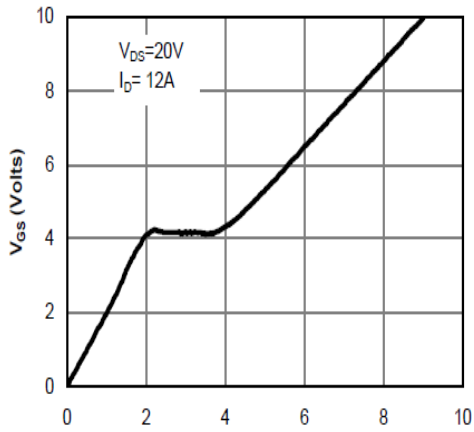


Figure 11. Gate Charge

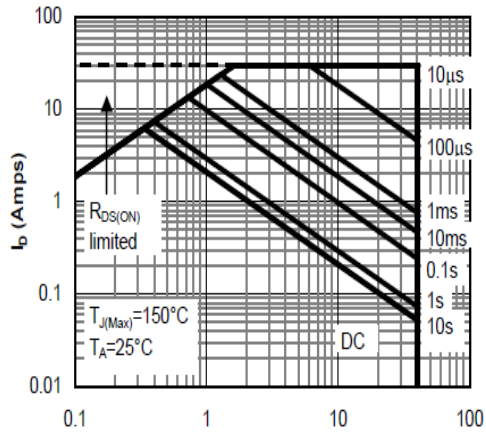


Figure 12. SOA, Safe Operation Area

## Typical Characteristics ( $T_J=25^\circ\text{C}$ Noted)

## P-Channel

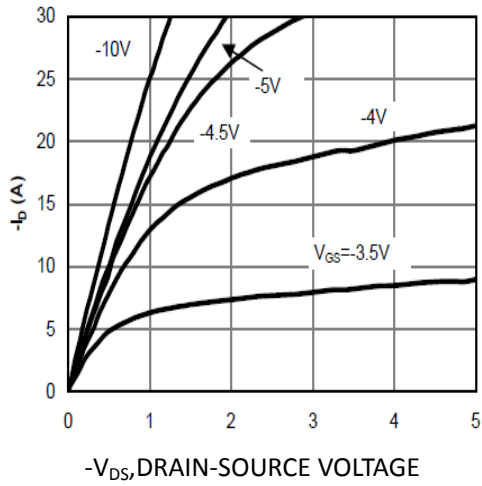


Figure 13. Typical Output Characteristics

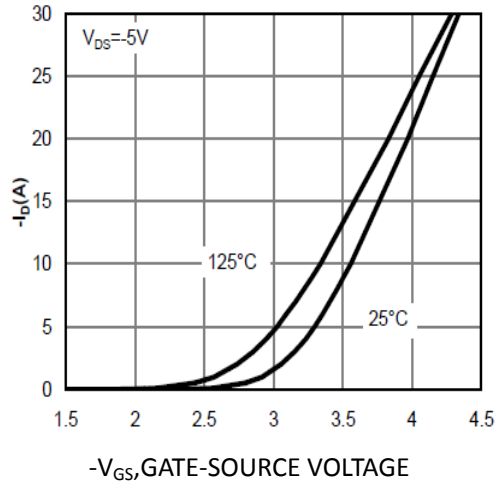


Figure 14. Typical Transfer Characteristics

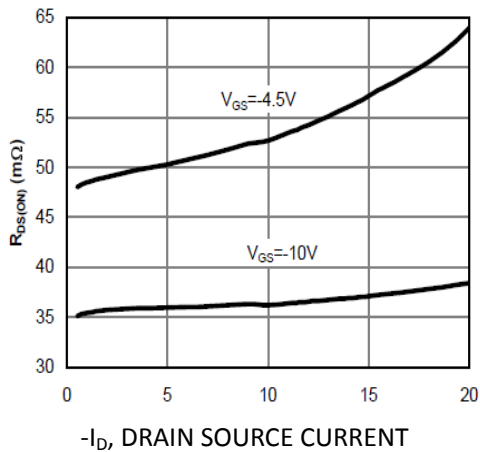


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

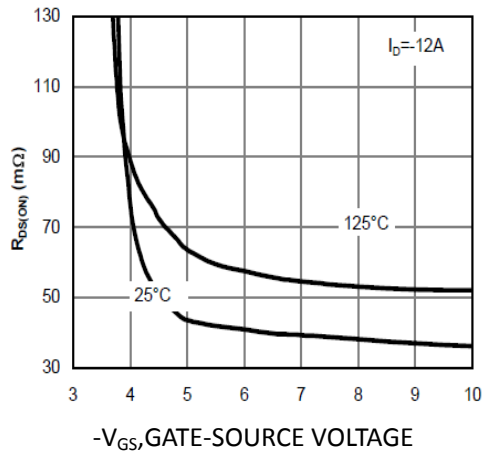


Figure 16. Typical On-Resistance vs. Drain Current and Gate Voltage

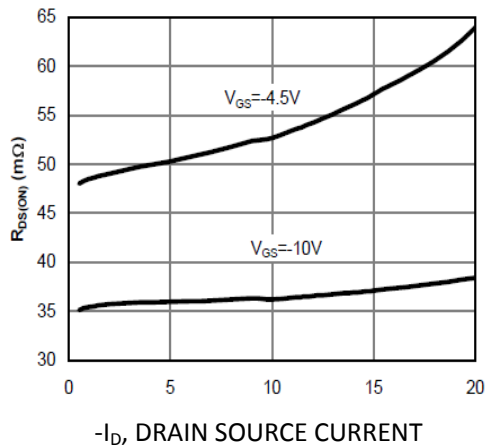


Figure 17. Typical On-Resistance vs. Drain Current and Temperature

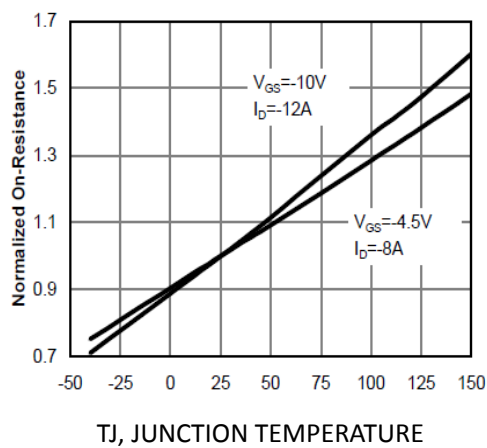


Figure 18. On-Resistance Variation with Temperature

## Typical Characteristics ( $T_J=25^\circ\text{C}$ Noted)

## P-Channel

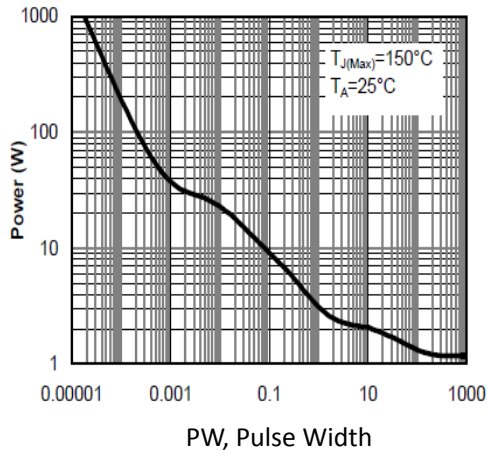


Figure 21. Single Pulse Power Rating  
Junction-to-Ambient

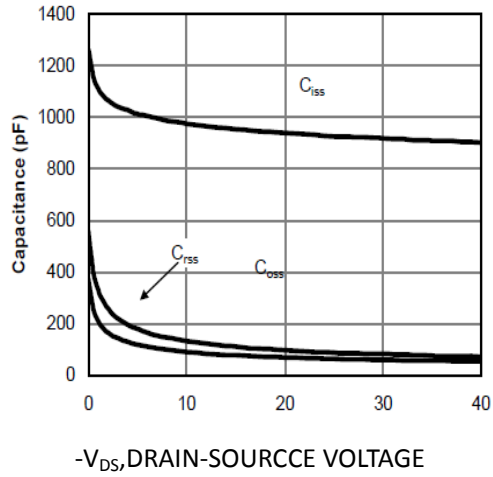


Figure 22. Typical Junction Capacitance

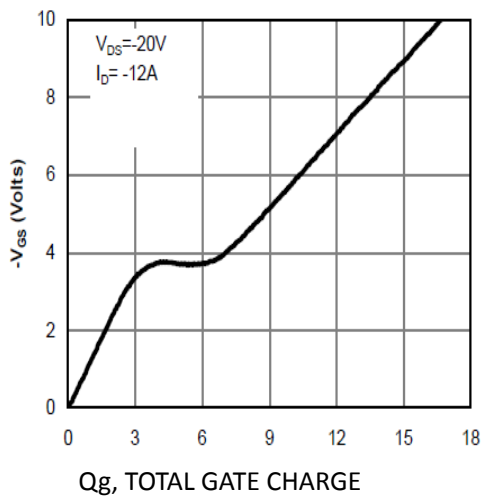


Figure 23. Gate Charge

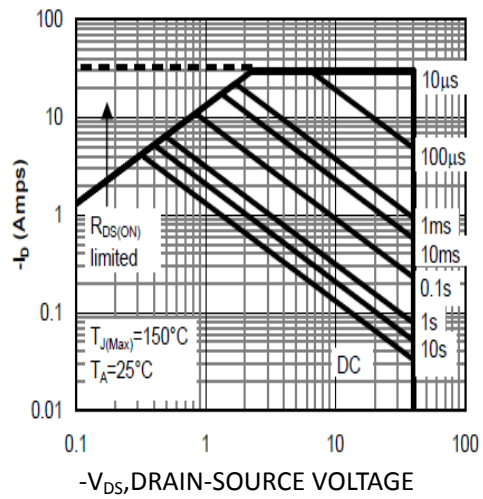
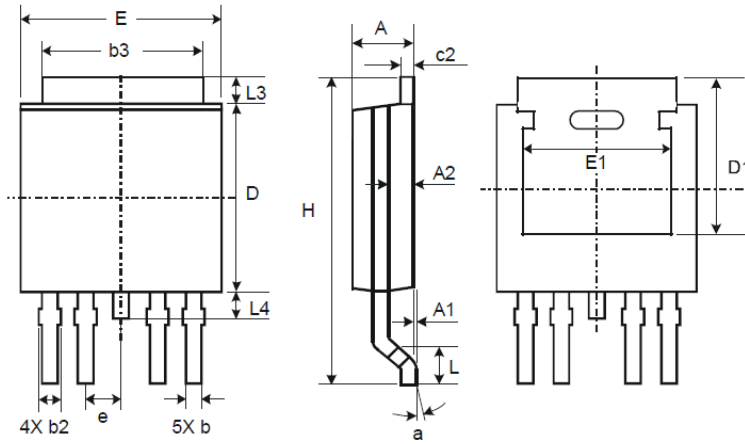


Figure 24. SOA, Safe Operation Area

## TO252-4L Package Outline



TO252-4L			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.51	0.71	0.583
b2	0.61	0.79	0.70
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	1.27
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			